YUKANG XIE

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Education

Wuhan University, Wuhan

Master of Engineering in Cyberspace Security

Huazhong University of Science and Technology, Wuhan

Bachelor of Engineering in Hydraulic and Hydro-Power Engineering

Research Experience

Reconfigurable Dataflow Architecture for Cryptography Processing

A crypto processing framework aiming both efficiency and flexibility, current work for master's thesis

- Integrating heterogeneous coarse-grained crypto operation units with on-chip networks.
- Designing a programming model and DSL for describing crypto protocol/algorithm in a dataflow manner.
- Mapping the programming model into a dataflow architecture to achieve reconfigurability.
- Tuning the performance of on-chip network with simulator and verificating the design through FPGA prototyping.

Virtualization Support of Symmetric Cipher Hardware Accelerators

Optimized architectures for AES and SM4, main designer and implementer

- Aiming to improve hardware utilization efficiency and enhance user experience in virtualized environments.
- Proposed schemes partition cipher modules' pipeline into independent units to enable parallel execution of tasks from different guests.
- $\ A chieved \ comparable \ throughput/area \ efficiency \ to \ previous \ work \ while \ supporting \ guest-level \ parallelization.$
- This work has been accepted by ICA3PP 2023 as regular paper.
- $\ The \ paper \ is \ under \ publishing. \ Preprint \ available \ at: \ \underline{https://easychair.org/publications/preprint/BNHg}.$

Personal Projects

WASM-PROCESSOR

A 3-stage pipelined WebAssembly processor, work in progress

- The design is implemented in Chisel HDL.
- Supports basic 32-bit instructions defined in WebAssembly spec, including arithmetic & logic operations, branches and function calls.
- Goal: Drawing practical conclusions on whether WebAssembly can be used as a reference for designing secure ISAs for microprocessors.
- The project has been open-sourced on GitHub: https://github.com/bathtub-01/wasm-processor.

Bathtub Thoughts (https://bathtub-01.github.io)

Personal tech blog

- Sharing knowledge from work experience and self-learning journey.

– Topics include PL theory, computer architecture and hardware development.

Skills & Interests

- **Programming Languages**: Working languages include C/C++, Python and Chisel HDL. Familiar with functional programming using Scala and Haskell.
- **FPGA Development**: Experienced in FPGA prototyping and verification for research purpose. Familiar with Xilinx FPGA toolchains.
- Cryptography: Knowledgeable about mainstream crypto algorithms and their mathematical foundation.
- **Computer Architecture**: Experienced in crypto accelerator and on-chip network design. Understand basic CPU design and other parallel architectures. Have experience in on-chip network simulator development.
- **Compiler**: Understand basic program representations and code optimization techniques. Basic experience in LLVM development.
- Areas of Interest: Computer architecture, functional programming and compiler optimization for DSLs.
- Languages: English (IELTS 7.5), Chinese (native).

Sept, 2021-June, 2024 (expected) Average Score: 87.52/100 Sept, 2017-June, 2021 Average Score: 80.4/100

2023-Present

2023-Present

2022-Present

2022-2023