Yukang Xie

PhD Researcher in Computer Architecture · Functional Languages · FPGA

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Research

Architectural Optimisation for Lazy Functional Language Processors *2025–2026*

- Designed a **pipelined, dataflow-driven processor** supporting automatic multithreading.
- Designed a companion **hardware garbage collector** with concurrent mark-and-sweep.
- Achieved up to **118% runtime improvement** over the single-cycle design, with zero measured GC overhead on general benchmarks.

Specialised Processor for Haskell Based on Structured Combinators *2024–2025*

- Designed a single-cycle stack machine for efficient combinator graph reduction, executing one structured combinator per cycle.
- Extended the **MicroHs** compiler with a new code-generation scheme for structured combinators.
- Achieved a minimal FPGA area footprint while reducing runtime by up to **58%** relative to SKI combinator schemes.

Reconfigurable Architecture for Cryptography Processing (Master's Thesis) *2023–2024*

- Integrated heterogeneous coarse-grained cryptographic operation units through on-chip networks.
- Designed a programming model and DSL for expressing cryptographic protocols and algorithms in a dataflow manner.
- Mapped DSL descriptions onto the architecture and tuned the on-chip network through simulation and FPGA prototyping.

Virtualisation Support for Symmetric-Cipher Hardware Accelerators *2022–2023*

- Designed schemes that partition AES/SM4 cipher pipelines into independent units for parallel execution of tasks from different guests.
- Supported guest-level parallelisation while retaining throughput/area efficiency comparable to prior work.

Selected Publications

- **ASAP 2026**. *Ouros: A Dataflow-Driven Processor for Lazy Functional Programming Languages*.
- **TFP 2025**. *From Haskell to a New Structured Combinator Processor*.
- **ICA3PP 2023**. *A Pipelined AES and SM4 Hardware Implementation for Multi-Tasking Environments*.

Education

Heriot-Watt University, Edinburgh *Sep 2024–Present*
PhD in Computer Science

Wuhan University, Wuhan *Sep 2021–Jun 2024*
MEng in Cyberspace Security GPA: 87.52/100

Huazhong University of Science and Technology, Wuhan *Sep 2017–Jun 2021*
BEng in Hydraulic and Hydro-Power Engineering GPA: 3.41/4.00

Technical Skills

Programming: Haskell, Rust, Scala/Chisel HDL (happier with functional programming, but comfortable with other languages)
Hardware : Simulator implementation, FPGA prototyping and verification, Xilinx FPGA toolchains
Architecture : Functional-language processors, cryptographic accelerators, on-chip networks, CGRAs, conventional CPU microarchitecture
Verification : Hardware correctness model checking with Kind 2
Languages : Chinese (native), English (IELTS 7.5)